A SIMPLE POST-FILTER FEEDBACK TOPOLOGY FOR CLASS-D AMPLIFIERS

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A feedback topology shall be proposed that allows the straightforward inclusion of the output filter into the feedback loop. It can be adapted to high- or low- Q output filters equally well. It is not restricted to either self-oscillating or carrier – based modulator topologies. One advantage is that the slew-rate requirements on the operational-amplifiers used for the proposed topology are quite relaxed since they are not forced to handle fast transients. Another advantage is that the feedback branch is based on resistors only.

INTRODUCTION

There are still a lot of class-d amplifiers being developed today that don't use post-filter feedback - despite advantages like better load independence of the frequency-response and reduction of the nonlinear distortion introduced by the output filter's nonlinearities. One of the main reasons for this situation is that some of the usual post-filter NFB topologies may either be too complicated to design, are lacking stability, or are only applicable to one type of modulator (like self-oscillating for instance). The topology proposed here is easy to design, showing good load-independency and can be applied to either carrier-based or self-oscillating class-d topologies.

1 FIRST ORDER PRE-FILTER NFB

One of the earliest commercially available class D amplifiers was based on the Japanese patent [1]. The basic topology is shown by (Fig 1).

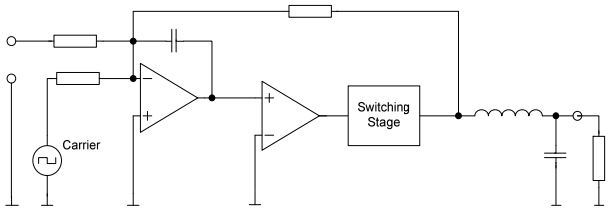

Figure 1: A very basic first-order loop topology with pre-filter feedback takeoff.

Alternatively to using a fixed-frequency carrier various self oscillating modulator topologies can be built. The self-oscillation can either be generated by phase shift or by the use of a Schmitt trigger in the modulator stage. The application note [2] is showing one such example.

There are sources that recommend the use of a loop filter of the form shown by Equation 1 - also known as PT1 - instead of an integrator.

$$F_{loop}(s) = A\frac{1}{1+sT_L} \tag{1}$$

The reason for this is either achieving a (subjectively) more naturally sounding amplifier [4] or the need for quick recovery from clipping [5]. Reasonable open-loop pole frequencies would lie between 5 kHz and 20 kHz.

The disadvantage of these very simple first-order loops is that they don't allow taking the negative feedback from the output of the reconstruction filter due to stability issues (i.e. insufficient phase margin). The load-dependant frequency response of the output LC filter and magnetic nonlinearities of the filter coil's ferromagnetic core however ask for the feedback to be taken from the output of the filter.

2 SOME EXISTING TOPOLOGIES

Let's first have a look at some known topologies for post-filter feedback.
A well-known circuit to build 2nd order control-loops is the PID controller (Fig. 2).

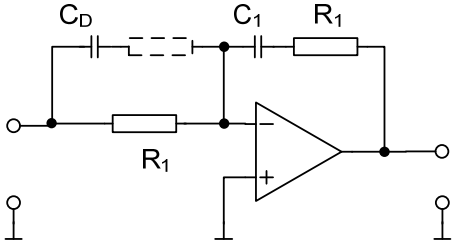

Figure 2: The PID controller .

Its transfer function is given by Equation 2.

$$F_{PID}(s) = -\frac{R_2}{R_1}\left[1 + (sC_D R_1 - \frac{1}{sC_I R_2})\right] \quad (2)$$

While having the advantage of being quite simple - it doesn't allow to completely compensate a 2nd order low pass function within the loop when said low pass is having a Q value higher than 0.5.

Another known circuit topology that is sometimes used in feedback control is the so-called PD2. While this would perform the compensation of any imaginable 2nd order low pass function (including high Q-values) - it has its own issues like increased component count and the use of double differentiation in an EMC-critical environment.

A quite sophisticated post-filter feedback topology is presented by [3].

A further example that is using a simple and elegant self-oscillating post-filter loop topology is shown by [4].

3 THE NEW LOOP TOPOLOGY

3.1 Derivation

The two main requirements for the circuit were that its total loop transfer function is following Equation 1 and that there were no other components than resistors allowed in the feedback path.

The amplifier will have a second order output filter whose transfer function is defined by Equation 3.
So we want to find the function $F_x(s)$ that will result in our PT1 function from Equation 1 when multiplied with the 2nd ord output filter's transfer function F_{filt} as shown by Equation 3.

$$F_{filt}(s) = \frac{1}{1 + sT_F / Q_F + s^2 T_F{}^2} \quad (3)$$

$$A\frac{1}{1+sT_L} = f_x * \frac{1}{1 + sT_F / Q_F + s^2 T_F{}^2} \quad (4)$$

Rearranging Equation 4 is leading to Equation 5 while at the same time intentionally omitting the gain factor A. This way only the frequency – dependant part is derived here. The constant gain factor A can easily be introduced again later on.
This can be further rearranged into Equation 6.

We will thus arrive at the sum of three elements namely a low pass (i.e. PT1) and a high pass and yet another high pass multiplied with a differentiator like as shown by Equation 6.

$$f_x = \frac{1}{1+sT_L} * (1 + sT_F / Q_F + s^2 T_F{}^2) \quad (5)$$

$$f_x = \frac{1}{1+sT_L} + \frac{sT_F / Q_F}{1+sT_L} + \frac{s^2 T_F{}^2}{1+sT_L} \quad (6)$$

Another rearrangement, leading to Equation 7 shows that the high pass is only needed once.

$$f_x = \frac{1}{1+sT_L} + \frac{sT_L}{1+sT_L}\left(\frac{T_F}{Q_F * T_L} + sT_L \frac{T_F{}^2}{T_L{}^2}\right) \quad (7)$$

A possible block diagram achieving the desired transfer function may look like shown in (Fig 3).

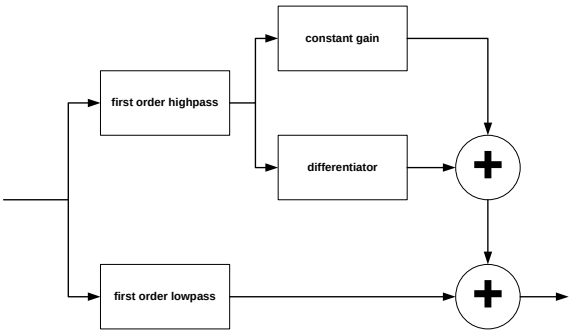

Figure 3: Building blocks of the loop transfer function.

A simple embodiment of the topology is shown by (Fig. 4). There are many possible solutions to implement the desired loop function of course.
The impedance relationships have to be suitably chosen to get this simple version proposed here working properly. Otherwise a buffer would be needed after the 1st order high pass formed by C_H and R_H.

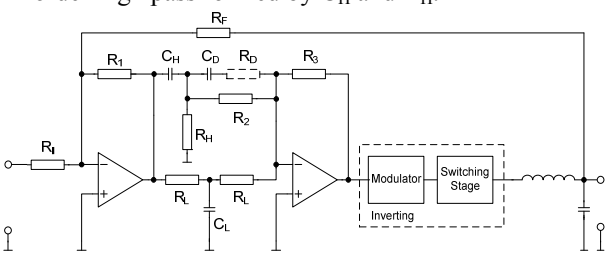

Figure 4: A possible implementation of the proposed loop filter topology.

$$A_{Loop} = -\frac{R_1 R_3}{R_F}\left(\frac{1}{2R_L}\frac{1}{1+s0.5R_L C_L} + \frac{s\dfrac{R_H R_2}{R_H+R_2}C_H}{1+s\dfrac{R_H R_2}{R_H+R_2}C_H}\left(\frac{1}{R_2}+sC_D\right)\right) * A_{HS} * F_{filt}(s) \approx -\frac{R_1 R_3}{2R_F R_L} * \frac{1}{1+s0.5R_L C_L} \quad (8)$$

$$A_F = -\frac{R_1 R_3}{R_I}\left(\frac{1}{2R_L}\frac{1}{1+s0.5R_L C_L} + \frac{s\dfrac{R_H R_2}{R_H+R_2}C_H}{1+s\dfrac{R_H R_2}{R_H+R_2}C_H}\left(\frac{1}{R_2}+sC_D\right)\right) * A_{HS} * F_{filt}(s) \approx -\frac{R_1 R_3}{2R_I R_L} * \frac{1}{1+s0.5R_L C_L} \quad (9)$$

The loop gain is determined by Equation 8 where $F_{filt}(s)$ is the transfer function of the output filter and A_{HS} is the gain of the modulator/switching-stage combination. The forward transfer function is given by Equation 9.

For frequencies below the unity-gain point the closed-loop gain A_{cl} of the complete amplifier is given by Equation 10.

$$A_{cl} \approx -\frac{R_F}{R_I} \quad (10)$$

The circuit can easily be adapted to different supply voltage and/or closed-loop gain simply by changing R_I and R_F while keeping the loop transfer function as originally designed.
If a PID controller was used, for instance, at least one capacitor in the feedback branch would have to be changed as well (which itself - unfortunatley - would often be of the ceramic type due to the low capacitances involved).
The most similar prior art that could be found so far is Figure 19 in patent [6] - although that topology's loop gain reaches its maximum at the output filter's cut-off frequency and doesn't increase further below that point.

3.2 Increasing the loop order

Although the distortion performance of second-order feedback loops isn't improved much over that achieved by a first-order loop [7] there is sometimes the need to increase the loop gain further in order to improve damping factor and/or PSRR.

The loop order of the circuit shown by (Fig. 4) can easily be increased to second order, by changing the feedback loop around the first operational amplifier, such that it is working as a lag filter. This is shown by (Fig.5) with the lag function formed by R_1, C_Z and R_Z. Alternatively the lag filter can be built around the second OP-AMP as well.

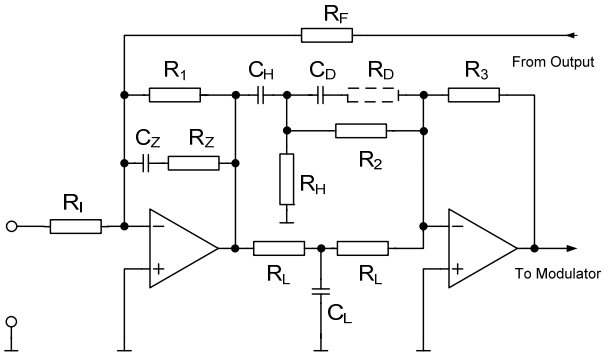

Figure 5: Increasing the loop order to 2nd order.

3.3 Symmetrical implementation

Papers [4] and [8] recommend the symmetrical implementation of a class-d amplifier's feedback loop in order to reduce EMC problems.
Since any nonlinear distortion originating from the feedback-path is not reduced by the loop, any components that are prone to nonlinearity should best be avoided there.
Therefore the use of an op-amp based differential amplifier for feedback-takeoff is not recommended.
Active parts should thus only be used in the forward path of the amplifier.

One possible example how the circuit from (Fig. 5) could be implemented in symmetrical fashion is shown by (Fig. 6) for a carrier-based PWM amplifier.

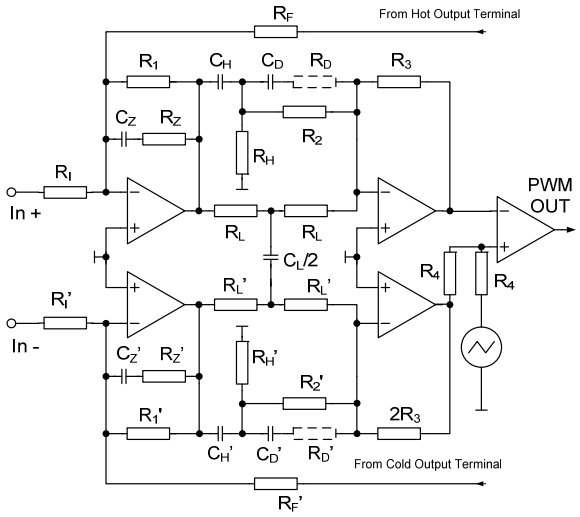

Figure 6: Symmetrical implementation of the 2nd order loop topology.

3.4 How to make the best use of the "improved" bandwidth

The fact that the feedback loop is first order and the feedback path is purely resistive could lead to the assumption that we now have a high-bandwidth amplifier, with a linear amplitude response up to the unity-gain frequency.
But both the power bandwidth (restricted by the output filter) and the sampling theorem will not let this happen. Although the small-signal bandwidth may be higher than that of the output filter, one is definitely running into TIM or aliasing problems sooner or later when trying to take advantage of the high small-signal bandwidth.
It should be noted however that there are in fact topologies which might profit from the increased small-signal bandwidth without increased risk of TIM distortion: Feed forward error correction, additional feedback loops, current loops used for influencing the parameters of loudspeaker drivers or also motional feedback just to name a few.
But it is definitely advisable to use an input lowpass filter for this amp topology.
One of the main points of criticism against class-d amplifiers is the restricted bandwidth compared to conventional linear amplifiers.
On the other hand one has to ask why an amplifier should have a bandwidth that is much higher than the audible range. In the author's opinion the only rational reason for having high upper cutoff frequencies is to keep group-delay distortion at the upper end of the audio range as low as possible. From the bandwidth point-of view alone an upper cutoff frequency around 40 kHz should be sufficient for most purposes.
By the use of well-known phase equaliser techniques (using higher order all-pass filters) a flat-group delay response could be achieved that is linear beyond the amplifier's cutoff frequency - at the expense of a slightly increased total group-delay. When applied to active speaker systems even the phase response of the tweeter could be taken into account and therefore a combined system group-delay performance could be achieved that rivals what can be achieved with even the highest-bandwidth conventional amplifiers available.

4 A DESIGN EXAMPLE

The following example shall show how the components of the loop are calculated and how the frequency response will look like. We will therefore design a hypothetical carrier-based amplifier with the following base-data: Closed-loop gain = -1, f_L = 10 kHz, output-filter pole frequency f_F = 40 kHz, output-filter Q = 1, nominal load impedance = 6 Ω and unity-gain point f_T = 120 kHz (this would be suitable for a carrier frequency of 384 kHz for instance). The gain of the hypothetical modulator/switching-stage combination is assumed to be -1 (like it would be achieved using a triangle with an amplitude of 1 V and a switching stage with a supply voltage of ± 1 V for instance).

The DC gain of the loop is given by Equation 10 wich can be followed from Equation 8.

$$A_{loop} = \frac{f_T}{f_L} = \frac{R_1 R_3}{2 R_F R_L} \qquad (10)$$

With the given values for f_T and f_L we get a DC- gain of 12. This can be achieved with reasonable accuracy using the following standard resistor values:

R_1 = 12.0 k Ω
R_3 = 4.7 k Ω
R_F = 2.2 k Ω
R_L = 1.0 k Ω

The other component values can be determined using Equations 11 to 14. R_H is chosen such that it is resonably smaller than R_2 (and also such that C_H has a reasonable value for the given f_L).

$$C_L = \frac{1}{2\pi f_L 0.5 R_L} \quad (11)$$

$$R_2 = 2R_L \frac{Q_F f_F}{f_L} \quad (12)$$

$$C_H = \frac{R_H + R_2}{2\pi f_L R_H R_2} \quad (13)$$

$$CD = \frac{1}{4\pi f_L R_L}\left(\frac{f_L}{f_F}\right)^2 \quad (14)$$

The rest of the chosen component values are therefore:

R_H = 1.8 k Ω
R_2 = 8.2 k Ω
C_L = 33 nF
C_H = 10 nF
C_D = 520 pF

The closed loop gain was chosen to be -1 therefore $R_I = R_F$.
The purpose of resistor R_D is to counteract the non-ideal lowpass behaviour of real-world LC output filters: The parasitic series inductance of capacitors and the parasitic parallel capacitance of inductors cause the lowpass to loose its effectiveness at frequencies in the MHz range. Therefore the overall loop function wouldn't be a first order lowpass anymore.
If using an R_D is insufficient and there is the need for one or two more lowpass poles at high frequencies capacitors in parallel with R1 and/or R3 can be used.

(Fig. 7 a & b) show the open- and closed- loop gain into the nominal load. The closed-loop response clearly follows the predicted first-order low pass function having a cutoff frequency equal to the unity-gain point at 120 kHz. The overall open-loop response is reasonably close to the desired first-order lowpass function with a pole frequency of 10 kHz. The loop has a phase-margin of 90 degrees.

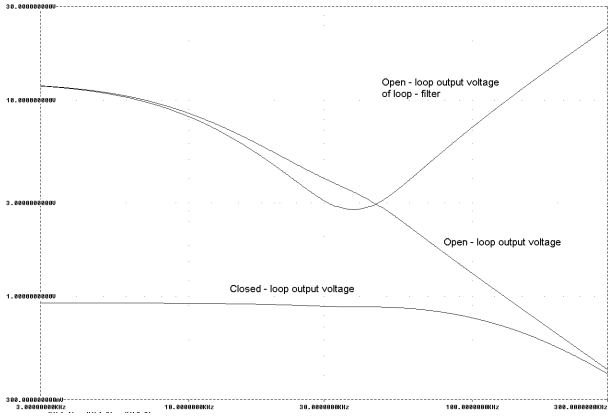

Figure 7a: Open- and closed-loop response into nominal load, amplitude response

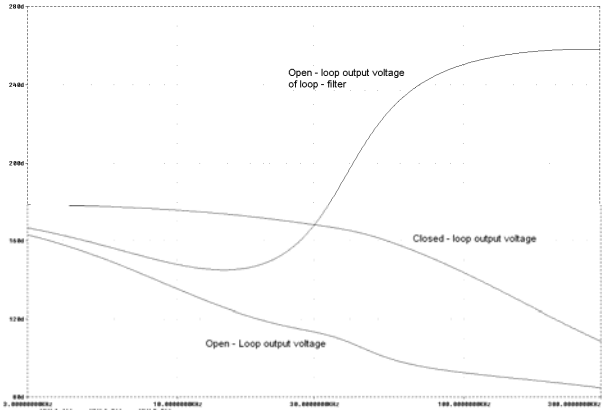

Figure 7b: Open- and closed-loop response into nominal load, phase response

(Fig. 8) Shows the closed loop gain for 2 Ω-, 4 Ω-, 8 Ω- and 16 Ω- loads. At low frequencies the amplitude-responses are equal. At very high frequencies they show to be asymptotically equivalent. It is the two-octave range above the output filter pole frequency where they differ the most - due to the decreasing loop-gain combined with the increased load dependancy of the output filter response around its pole frequency. Here the largest deviation is in the range of 8 dB. If the extremely low load of 2 Ohms isn't taken into consideration this is reduced to 4 dB approximately. Below 30 kHz however the difference between the responses is less than 0.5 dB.

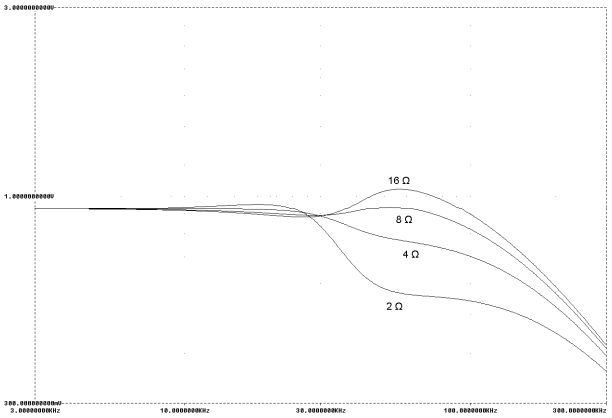

Figure 8: Output voltage into different loads

One possibility to improve on this is to use a higher switching frequency and therefore a higher unity-gain point. This would however mean to trade frequency - response linearity against efficiency. Wheter this is advisible has to be decided case by case.

5 CONCLUSION

The paper shows that it is possible to implement simple post-filter feedback topologies for class-d amplifiers that are easy to design, show good load behaviour and do at the same time put low demands on the components used in the linear circuit parts of such an amplifier.

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